

CLAIMS

What is claimed is:

1. A processor comprising:
 - a first local voltage regulator to be powered by a global voltage and to provide a first local voltage to power a first circuit of the processor; and
 - a second local voltage regulator to be powered by the global voltage and to provide a second local voltage to power a second circuit of the processor.
2. The processor of claim 1, wherein the first and second voltages are independently adjustable by the processor.
3. The processor of claim 2, wherein the first voltage regulator includes a digitized resistor to be set by the processor.
4. The processor of claim 1, wherein the first local voltage is to be set to allow the first circuit to meet a timing requirement.
5. The processor of claim 1, wherein the first local voltage is to be reduced independent of the second local voltage if the first circuit is inactive and the second circuit is active.

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- 1 12. The computer system of claim 9, wherein the local supply voltages are to be
2 set to allow the processor to meet a timing requirement.
- 1 13. The computer system of claim 9, wherein each of the local voltage regulators
2 includes an op amp.
- 1 14. The computer system of claim 9, wherein the local supply voltages include
2 first and second supply voltages to power first and second circuits,
3 respectively, the first supply voltage to be reduced independent of the second
4 supply voltage if the first circuit is inactive and the second circuit is active.
- 1 15. A method comprising:
2 enabling a processor to receive a global Vcc and to provide a first local
3 Vcc and a second local Vcc to power first and second circuits,
4 respectively, of the processor; and
5 enabling the processor to independently adjust the first local Vcc and the
6 second local Vcc according to a power management policy.
- 1 16. The method of claim 15, wherein independently adjusting the first local Vcc
2 and the second local Vcc includes reducing the first local Vcc, independent of
3 the second local Vcc, if the first circuit is inactive.

1 17. The method of claim 15, further comprising setting the first local Vcc to allow
2 the first circuit to meet a first timing requirement.

1 18. The method of claim 17, further comprising setting the second local Vcc to
2 allow the second circuit to meet a second timing requirement, the first local
3 Vcc to be different than the second local Vcc.

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